

99P3399

JP

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 11136954 A

(43) Date of publication of application: 21.05.99

(51) Int. Cl

~~H02M 7/527 2WP~~  
(H02M 7/48)

(21) Application number: 09295560

(71) Applicant: YASKAWA ELECTRIC CORP

(22) Date of filing: 28.10.97

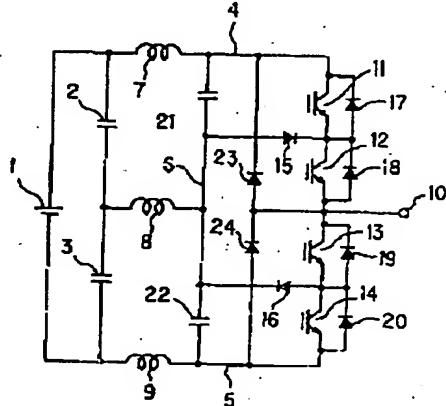
(72) Inventor:  
YAMANAKA KATSUTOSHI  
YAMADA KENJI  
KUMAGAI AKIRA  
TERADA TAKAAKI

(54) THREE-LEVEL NEUTRAL POINT CLAMP-TYPE  
INVERTER CIRCUIT

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a snubber function with less number of part items since providing an individual snubber circuit for each switching element is expensive and not economical.

SOLUTION: A three-level neutral point clamp-type inverter circuit, where a positive bus 4, a negative bus 5, and a neutral line 6 are provided, and first and second IGBTs 11 and 12 and/or third and fourth IGBTs 13 and 14 are connected in series between the positive bus 4 and a phase voltage output terminal 10 and/or the negative bus 5 and the phase voltage output terminal 10, respectively, first and second snubber capacitors 21 and 22 are provided between the positive bus 4 and the neutral line 6 and between the negative bus 5 and the neutral line 6, respectively, and first and second snubber diodes 23 and 24 are provided, where a cathode is connected to the positive bus 4 and an anode is connected to the phase voltage output terminal 10 in the first snubber diode 23, and the anode is connected to the negative bus 5 and the cathode is connected to the phase voltage output terminal 10 in the second snubber diode 24.



COPYRIGHT: (C)1999,JPO